UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/039,016	01/02/2002	Robert C. Glenn	42390P12278	7520

8791 7590 04/11/2006

BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES, CA 90025-1030

EXAMINER	
TRAN, KHANH C	

ART UNIT	PAPER NUMBER
2611	

DATE MAILED: 04/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/039,016	GLENN ET AL.	
	Examiner	Art Unit	
	Khanh Tran	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,6,9-19 and 21-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *9-16* is/are allowed.

6)☒ Claim(s) *1,3,17,18,25 and 27* is/are rejected.

7)☒ Claim(s) *6,19,21-24 and 26* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 July 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The Amendment filed on 01/19/2006 has been entered. Claims 1, 3, 6, 9-19 and 21-27 are pending in this Office action.

Response to Arguments

2. Applicant's arguments with respect to claims 17 and 25 have been considered but are moot in view of the new ground(s) of rejection. See Explanation in claim rejection below.

3. There is a typographical error in referring Buchwald et al. reference as U.S. Patent 6,509,733 B2 in the last Office action. The correct U.S. Patent Number should be U.S Patent 6,509,773 B2.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 17-18 are rejected under 35 U.S.C. 102(e) as being anticipated by Buchwald et al. U.S Patent 6,509,773 B2.

Regarding claim 17, referring to figure 3, in column 9 lines 3-67, Buchwald et al. teaches a timing recovery module 202 receiving a serial data signal 104, the timing recovery module 202 comprising:

- In column 9, lines 55-67, Buchwald teaches that phase detector 312 (see figure 3) detects a phase error 350 between data sampling signal 208 and serial data signal 104 based on the data samples in data signal 346 and the phase samples in phase signal 348. The data sampling signal 208 is also a timing signal; see column 9, lines 25-30. In view of the aforementioned teachings, the data-sampling signal 208 corresponds to the claimed recovered clock signal.
- A phase controller 302 produces a plurality of digital control signals 340, which correspond to the claimed interrelated control signals. Therefore, the phase controller 302 generates plurality of digital control signals 340 based on the comparison between data sampling signal 208 and serial data signal 104 as recited above.
- a phase interpolator 306 coupled with the phase controller 302 producing timing/sampling signal 208 and a second timing/sampling signal 344 offset in phase from sampling signal 208, based on reference signal set 206 and a plurality of digital control signals 340 applied to the phase interpolator.

- On page 9 of Applicants' Remarks, Applicants argue that Buchwald does not teach or suggest a phase interpolator that can change the phase of a recovered clock signal with an analog transition. The Examiner responds that Applicants' arguments are not persuasive for the following reasons. Figure 8 illustrates a phase interpolation environment 800 including a phase interpolator 801 (such as phase interpolator 306 shown in figure 3), and a stage controller 806 (such as phase control rotator 304 shown in figure 3); see column 13 lines 55-65. In column 14 lines 26-40, the output signal 826 of the phase interpolation environment 800 is a *periodic waveform* [Emphasis added]. Furthermore, referring to figure 8, in column 14 lines 5-25, Buchwald teaches that each reference stage 802 generates a component signal 824 from its corresponding reference signal 822 according to a scaling factor that is the ratio of a component signal 824 magnitude to its corresponding reference signal 820 magnitude. A reference stage 802 scaling factor is determined by its corresponding control signal 822. Component signals 824 are each sent to combining node 804. Combining node 804 combines each of component signals 824 to produce an output signal 826. This combining includes summing each of the individual component signals 824 (some of which may have a magnitude equal to zero). As a result of this combining, output signal 826 is a periodic waveform having a phase that is derived from the phases of component signals 824. In view of

Buchwald disclosure, output 208 of the phase interpolator 306, corresponding to the claimed recovered clock signal, is generated from the analog transition of periodic reference signals.

Regarding claim 18, in column 13 lines 1-20, phase error processor 314 asserts, based on the phase control commands 354, the phase-hold command when sampling signal 208 and serial data signal 104 are phase aligned with one another; the phase-retard command when the phase of sampling signal 208 leads the phase of serial data signal 104; and the phase-advance command when the phase of sampling signal 208 lags the phase of serial data signal 104. In view of the foregoing, the phase-retard command and the phase-advance command correspond to the claimed charge and discharge signals.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 3, 25 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Buchwald et al. U.S Patent 6,509,773 B2.

Regarding claim 1, referring to figure 3, in column 9 lines 3-67, Buchwald et al. teaches a timing recovery module 202 comprising:

- a phase controller 302 including data path 308, a phase path 310, a phase detector 312 coupled to the data and phase paths, and a phase error processor 314 coupled to the phase detector; see column 9, lines 4-67. The phase controller 302 produces a plurality of digital control signals 340, which correspond to the claimed interrelated control signals.
- In column 9, lines 55-67, Buchwald teaches that phase detector 312 (see figure 3) detects a phase error 350 between data sampling signal 208 and serial data signal 104 based on the data samples in data signal 346 and the phase samples in phase signal 348. The data sampling signal 208 is also a timing signal; see column 9, lines 25-30. In view of the aforementioned teachings, the data-sampling signal 208 corresponds to the claimed recovered clock signal. Therefore, the phase controller 302 generates plurality of digital control signals 340 based on the comparison between data sampling signal 208 and serial data signal 104 as recited above. Buchwald et al. differs from the pending application in that Buchwald et al. teaches the phase detector 312 being inside the phase controller 302. Nevertheless, because the phase detector 312 and the phase controller 302, as taught by Buchwald, perform equivalent function, one of ordinary skill in the art at the time the invention was made would have recognized the interchangeability of Buchwald teachings for phase-frequency detector and phase controller specified in the pending claim.

- In column 13 lines 1-20, phase error processor 314 asserts, based on the phase control commands 354, the phase-hold command when sampling signal 208 and serial data signal 104 are phase aligned with one another; the phase-retard command when the phase of sampling signal 208 leads the phase of serial data signal 104; and the phase-advance command when the phase of sampling signal 208 lags the phase of serial data signal 104. In view of the foregoing, the phase-retard command and the phase-advance command correspond to the claimed charge and discharge signals. The phase error processor 314 corresponds to the claimed phase update logic circuitry.
- a phase interpolator 306 coupled with the phase controller 302 producing timing/sampling signal 208 and a second timing/sampling signal 344 offset in phase from sampling signal 208, based on reference signal set 206 and a plurality of digital control signals 340 applied to the phase interpolator.
- Furthermore, the phase interpolator 306 also receives a plurality of digital control signals 340 generated by the controller 302. As result of that, the amplitude contributions from more than one phase are weighted in accordance with the plurality of digital control signals 340. Figure 8 illustrates a phase interpolation environment 800 including a phase interpolator 801 (such as phase interpolator 306 shown in figure 3), and a stage controller 806 (such as phase control rotator 304 shown in figure

3); see column 13 lines 55-65. In column 14 lines 26-40, the output signal 826 of the phase interpolation environment 800 is a *periodic waveform* [Emphasis added]. Furthermore, referring to figure 8, in column 14 lines 5-25, Buchwald teaches that each reference stage 802 generates a component signal 824 from its corresponding reference signal 822 according to a scaling factor that is the ratio of a component signal 824 magnitude to its corresponding reference signal 820 magnitude. A reference stage 802 scaling factor is determined by its corresponding control signal 822. Component signals 824 are each sent to combining node 804. Combining node 804 combines each of component signals 824 to produce an output signal 826. This combining includes summing each of the individual component signals 824 (some of which may have a magnitude equal to zero). As a result of this combining, output signal 826 is a periodic waveform having a phase that is derived from the phases of component signals 824.

Regarding claim 3, in column 12 lines 40-65, Buchwald et al. teaches that at next step 712, phase detector 312 derives phase error signal 350 indicative of whether each data sample time t_d is early or late with respect to the optimum symbol sample time t_0.

Regarding claim 25, claim 25 is rejected on the same ground as for claim 1 because of similar scope.

Regarding claim 27, referring to figure 8, in column 14 lines 5-30, Buchwald et al. teaches that interpolator 801 includes a plurality of reference stages 802a-d that are each coupled to stage controller 806, and a combining node 804 that is coupled to each of reference stages 802. The stage controller 806 corresponds to the claimed phase control circuitry and control signals 822 (see figure 8) correspond to the claimed interrelated control signals. Referring to figure 11, in column 15 lines 55-65, FIG. 11 is an exemplary schematic of a reference stage 802 circuit that receives a binary control signal 822. In column 16 lines 15-25, the flow of current 1128 enables reference signal 820 to be converted into corresponding component signal 824. That is, source current 1128 enables the conversion of differential reference signals 1120 and 1122 into differential component signals 1124 and 1126, respectively.

Allowable Subject Matter

6. Claims 6, 19, 21-24 and 26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. Claims 9-12 are allowed.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 9, claim is allowed because Applicants amended claim to include allowable limitations "*wherein said phase controller comprises a first phase control circuit to generate a first interrelated control signal of the interrelated control signals and a second phase control circuit to generate a second interrelated control signal of the interrelated control signals, wherein the second interrelated control signal decreases in amplitude at substantially the same rate as the first interrelated control signal increases in amplitude*".

8. Claims 13-16 are allowed.

The following is a statement of reasons for the indication of allowable subject matter:

Regarding claim 13, claim is allowed because Applicants amended claim to include allowable limitations "*wherein said phase controller further comprises common mode feedback circuitry coupled with more than one phase control circuit to substantially compensate for changes in a common mode amplitude of managing interrelated control signals of the interrelated control signals*".

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khanh Tran whose telephone number is 571-272-3007. The examiner can normally be reached on Monday - Friday from 08:00 AM - 05:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on 571-272-2988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KCT

Khanh Cong Tran 04/07/2006

Primary Examiner KHANH TRAN